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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,505	05/11/2004	Leo Wang	LKSP0030USA	3504

27765 7590 09/15/2005

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,505	WANG ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated August 31, 2005, Applicant has canceled Claims **1-11** and elected Invention II (Claims **12-20**), drawn to a device to be examined. Accordingly, Claims **12-20** are currently pending in the application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in TAIWAN, 092130992 on 11/05/2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **12, 14 and 17-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 5 Prior Art, Applicant's admitted prior art (AAPA) in view of Mori (USP 5,208,174).

Regarding claims **12, 14 and 17-19**, Fig. 5 Prior Art (AAPA) discloses and the corresponding texts as set forth in Description of the Prior Art, a flash memory cell comprising:

a substrate 42;

a stacked gate structure 50 positioned on the substrate, wherein the stacked gate structure from bottom to top comprises a tunneling oxide 53, a floating gate 54, an insulating layer 55, and a control gate 56;

a first conductive P-type shallow doped region 51 positioned in the substrate under the stacked gate structure;

a first conductive P-type deep region 52 positioned in the substrate at one side of the stacked gate structure;

a second conductive N-type drain doped region 46 positioned in the substrate at a same side with the deep doped region, a bottom and sidewalls of the drain doped region being surrounded by the deep doped region; and

a second conductive N-type source doped region 48 positioned in the substrate at an opposite side of the stacked gate structure.

Fig. 5 Prior Art (AAPA) fails to teach the floating gate and the control gate having an insulating barrier layer with rounded edges. However, Mori teaches in Fig. 2D that a flash memory cell/a nonvolatile semiconductor memory device comprises a floating gate 105 and a control gate 106 having an insulating barrier layer including a silicon oxidation film 108 and a thermal oxidation film 109 with rounded edges. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of a nonvolatile semiconductor memory device comprising a floating gate and a control gate having an insulating barrier layer including a silicon oxidation film and a thermal oxidation film with rounded edges, as taught by Mori to incorporate into and modify Fig. 5 Prior Art (AAPA) to arrive the claimed

limitations in order to prevent the electrical charge from being moved out of the edge portion as set forth in column 3, lines 33-38.

Regarding claim **20**, Fig. 5 Prior Art (AAPA) discloses the drain doped region and the deep doped region are electrically connected together.

Claim **13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 5 Prior Art, Applicant's admitted prior art (AAPA) in view of Mori (USP 5,208,174) and further in view of Hsu et al. (US Pub. No. 2002/0113272 hereinafter referred to as "Hsu").

Fig. 5 Prior Art (AAPA) and Mori disclose all the above claimed limitations except for the substrate further comprising a second conductive type well. Hsu teaches in Fig. 2 a flash memory cell structure comprises a substrate including a second conductive N-type well 34, and the deep doped region 35, the drain doped region 36, and the source doped region 38 are positioned above the second conductive type well in order to reduce the operational voltage of the memory cell so that both the effects of low operational voltage and high density can be achieved (see par. [0013]-[0014]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of a substrate including a second conductive N-type well, and the deep doped region, the drain doped region, and the source doped region are positioned above the second conductive type well, as taught by Hsu to incorporate into and modify Fig. 5 Prior Art (AAPA) and Mori's structure to arrive the claimed limitations a substrate including a second conductive N-type well, and the shallow doped region, the deep doped region, the drain doped region, and the source doped region are positioned above the

second conductive type well in order to reduce the operational voltage of the memory cell so that both the effects of low operational voltage and high density can be achieved.

Claims **15 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 5 Prior Art, Applicant's admitted prior art (AAPA) in view of Mori (USP 5,208,174) and further in view of Hsieh et al. (USP 6,207,501 hereinafter referred to as "Hsieh").

Fig. 5 Prior Art (AAPA) and Mori disclose all the above claimed limitations except for the control gate further comprises a silicide layer thereon, and the stacked gate structure further comprises a TEOS layer thereon. Hsieh teaches in Figs. 2A-2E a flash memory cell in an area A comprises a second polysilicon layer/a control gate 122 including a layer of tungsten silicide 123 and a layer of TEOS 124 (col. 3, line 29-col. 4, line 13). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a flash memory cell comprising a control gate including a layer of tungsten silicide and a layer of TEOS, as taught by Hsieh to incorporate into and modify Fig. 5 Prior Art (AAPA) and Mori's structure to arrive the claimed limitations since it was known in the art that a silicide layer is used for increasing electrical conductivity, and the TEOS layer is used as a capping layer for protecting the device.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

09/14/05

Andy Huynh

Patent Examiner